

REMARKS

Applicants respectfully traverse and request reconsideration.

The drawings are objected to as allegedly failing to show a "high speed bus arbiter" and a "low bus speed arbiter". Applicants respectfully note that the drawings were previously corrected and respectfully point the Examiner to the after final response dated July 5, 2005. Since these corrections were previously made, Applicants respectfully request that the objection be withdrawn.

Claims 18-20 and 24-25 stand rejected under 35 U.S.C. §112, second paragraph as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. As to claim 18, it is alleged that the language "the low speed arbiter supports a lower bus rate than the high speed bus arbiter" is unclear. It is alleged that page 6 of the Specification teaches that it is "the high speed bus that supports the low bus rate and it is the high speed bus that supports the high bus rate.". Applicants are uncertain as to this statement. On page 6, second full paragraph, the Specification states that the PCI bus arbiter and the I/O controller 130 controls the lower speed PCI ports 131 connected to PCI bus 132. In the paragraph above, it states that the high speed arbiter is in the system/graphic controller 120 that interfaces to the I/O controller 130 and the external PCI port 125. As also shown, the PCI bus 124 is a higher speed bus than PCI bus 132. As such, Applicants respectfully submit that the claim language appears to have been misinterpreted.

Claims 18-20, 24 and 25 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Iachetta Jr. in view of Porterfield and Ajanovic, and Heil et al. This is a new ground of rejection. It is admitted that the Iachetta reference does not disclose, among other things, that the high speed arbiter may be included in the system controller or host bridge 640, and that the low

speed arbiter may be included in the I/O controller or PCI/PCI bridge 810. Applicants respectfully note also, however, that the claims require that the claimed high speed arbiter, which is part of the system controller, is also coupled to the input/output controller via a high speed bus. The office action does not address this specific claim language. Accordingly, the rejection should be withdrawn.

In any event, it is also noted that not only does the office action fail to address this language, but that the Iachetta reference teaches an opposite approach as admitted in the office action. The high speed bus arbiter 710 of Iachetta is not shown to be coupled to the PCI/PCI bridge 810, which coupling is required by the claim. In fact, the alleged system controller of Iachetta, namely host bridge 640 is also admitted as not including the claimed high speed arbiter which as claimed is also coupled to the input/output controller that includes a low speed bus arbiter. As such, since Iachetta does not teach, among other things, an I/O controller coupled to a high speed bus arbiter via a high speed bus, and since none of the other references are cited for such structure, Applicants respectfully submit that the claims are in condition for allowance.

Moreover, the office action alleges that the Porterfield and Ajanovic references, when combined, would render the claimed structure obvious. However, Applicants respectfully submit that the office action cannot overlook claim language as noted above in an effort to render the claims obvious.

The dependent claims add additional novel and non-obvious subject matter.

As to claim 24, Applicants again respectfully reassert the relevant remarks made above and as such, these claims are also in condition for allowance.

Claim 25 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Iachetta Jr. in view of Porterfield and Ajanovic, and Heil et al. as applied to claims 18-20 above and further

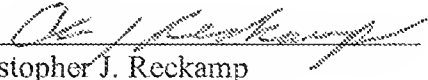
in view of "Wikipedia cited below". However, Applicants respectfully submit that there is no date given for the definition of Northbridge from Wikipedia and it is respectfully submitted that, as known in the art, Wikipedia is a website whose content is updated by many authors at different points in time. Applicants respectfully request a showing as to the date and content specifically relied upon in the office action if the claims are not allowed. Moreover, the claim requires a unified memory architecture wherein a unified memory is controlled to store both graphics data and system data in combination with the other language. Again, this subject matter has not been addressed in the office action and as such, the rejection should be withdrawn and the claims passed to allowance. However, if the rejection is maintained, Applicants respectfully request that all claim language be addressed in a non-final action.

The dependent claims add additional novel and non-obvious subject matter.

Accordingly, Applicants respectfully submit that the claims are now in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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